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TRANSMITTAL FORM (to be used for all correspondence after initial filing)			
		Application Number	09/912,231
		Filing Date	Jul 24, 2001
		First Named Inventor	Regula, Jack
		Art Unit	2112
		Examiner Name	Knoll, C.
Total Number of Pages in This Submission	83	Attorney Docket Number	136.1005.01

ENCLOSURES *(check all that apply)*

- [X] Fee Transmittal Form (2 copies)
  - [X] Fee Attached (PTO Form 2038 – 2 copies)
- [ ] Amendment / Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
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- [ ] After Allowance communication to Group
- [ ] Appeal Communication to Board of Appeals and Interferences
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Steven A. Swernofsky Reg. No. 33,040
Signature	SASwernofsky
Date	4-11-2005

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FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

[X] Applicant Claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 250.00

Complete if Known	
Application Number	09/912,231
Filing Date	7/24/2001
First Named Inventor	Regula, et al.
Examiner Name	Knoll, C.
Art Unit	2112
Attorney Docket No.	136.1005.01

METHOD OF PAYMENT *(check all that apply)*

[ ] Check [X] Credit card [ ] Money Order [ ] Other [ ] None

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Deposit Account Number: 50-0365

Deposit Account Name: Swernofsky Law Group PC

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FEE CALCULATION

1. BASIC FILING FEE

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1001	790	2001	395	Utility filing fee	
1002	350	2002	175	Design filing fee	
1003	550	2003	275	Plant filing fee	
1004	790	2004	395	Reissue filing fee	
1005	200	2005	100	Provisional filing fee	

SUBTOTAL (1) ($) 0.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra Claims		Fee from below		Fee Paid
Total Claims		-20**=		X		=	
Independent Claims		- 3**=		X		=	
Multiple Dependent						=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	50	2202	25	Claims in excess of 20
1201	200	2201	100	Independent claims in excess of 3
1203	360	2203	180	Multiple dependent claim, if not paid
1204	200	2204	100	**Reissue independent claims over original patent
1205	50	2205	25	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0.00

*** or number previously paid, if greater; For Reissues, see above*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge – late filing fee or oath	
1052	50	2052	25	Surcharge – late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	250.00
1403	1000	2403	500	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive – unavoidable	
1453	1,370	2453	685	Petition to revive – unintentional	
1501	1,400	2501	700	Utility issue fee (or reissue)	
1502	800	2502	400	Design issue fee	
1503	1,100	2503	550	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	790	2809	395	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR 1.129(b))	
1801	790	2801	395	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) ____________

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 250.00

SUBMITTED BY				Complete *(if applicable)*	
Name (Print/Type)	Steven A. Swernofsky	*Registration No. (Attorney/Agent)*	33,040	*Telephone*	650-947-0700
Signature	SA Swernofsky			*Date*	4-11-2005

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136.1005.01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:		Art Unit:	2112
	Jack REGULA *et al.*	Examiner:	Clifford H. KNOLL
Serial No.:	09/912,231	Tel:	(571) 272-3636
Filed:	July 24, 2001		
For:	ON-CHIP SWITCH FABRIC		

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APPEAL BRIEF TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

This Appeal Brief is responsive to the rejection mailed on November 12, 2004 in the above-referenced patent application. It is being filed within two months of the filing of a Notice of Appeal in this case. Therefore, the Appeal Brief is timely and no time extension fee is due. If the Applicants' attorney is mistaken in this regard, Applicants conditionally petition for an extension of time and authorization is hereby granted to charge all required time extension fees to Deposit Account No. 50-0365. Authorization is also granted to charge all other fees necessary to file this Appeal Brief, to the same Deposit Account.

04/15/2005 EFLORES 00000011 09912231
01 FC:2402 250.00 OP

I
REAL PARTY IN INTEREST

In this Appeal, the real party in interest is PLX Technology, Inc., a Delaware corporation, having a place of business at 870 Maude Avenue, Sunnyvale, CA 94085.

II
RELATED APPEALS AND INTERFERENCES

Appellants, Assignee, and the undersigned legal representative do not know of any other appeal, interference, or judicial proceeding that is related to, directly affects, is directly affected by, or has a bearing on the decision of the Board of Patent Appeals and Interferences (the "Board" or the "Board of Appeals") in this Appeal.

III
STATUS OF CLAIMS

The status of claims in the instant application is as follows:

Claims 1 through 42 have been rejected and are pending.

Applicants appeal from the rejection of claims 1-42.

IV
STATUS OF AMENDMENTS

Applicants filed a proposed amendment in response to the final Office action mailed on November 12, 2004 (the "Final Office Action" hereinafter). In advisory action mailed on February 4, 2005 (the "Advisory Action" hereinafter), Applicants were notified that the proposed amendment will not be entered. No amendments have been filed subsequent to the Advisory Action.

V
SUMMARY OF CLAIMED SUBJECT MATTER

A. Independent Claims

Claim 1

Claim 1 is directed to a system for communication on a chip, such as an integrated circuit chip. *E.g.,* specification at page 1, line 22 through page 2, line 3; *id.* at page 10, line 18.

The system includes an on-chip communication bus with plural tracks. *E.g.*, specification at page 10, lines 18-19; Figure 1, element 12. A track may include lines for data bits and control information. *E.g.*, specification at page 10, lines 1-4.

The system further includes a plurality of stations that couple a plurality of on-chip components to the on-chip communication bus. *E.g.*, specification at page 10, lines 19-20. A station is a port to the on-chip communication bus. *E.g.*, specification at page 8, line 7.

Each station has a dedicated track which it can use to send information to other stations. *E.g.*, specification at page 10, lines 20-21.

Claim 19

Claim 19 is directed to a method for communication on a chip. *E.g.*, specification at page 5, lines 17-18; *id.* at page 10, line 18; *id.* at page 20, lines 17-18.

The method includes a step of communicating between a plurality of on-chip components and a plurality of stations coupled to the plurality of on-chip components. *E.g.*, specification at page 4, lines 2-6; *id.* at page 5, lines 17-18; *id.* at page 20, lines 23-24; Figure 7, steps S701 and S709. A station is a port to an on-chip communication bus. *E.g.*, specification at page 8, line 7.

The method further includes a step of communicating between the plurality of stations using the on-chip communication bus including a plurality of tracks. *E.g.*, specification at page 4, lines 13-16; *id.* at page 5, lines 17-18; *id.* at page 10, lines 18-21; *id.* at page 20, line 24 through page 21, line 5; Figure 1, element 12. A track may include lines for data bits and control information. *E.g.*, specification at page 10, lines 1-4.

Each station has a dedicated track which it can use to send information to other stations. *E.g.*, specification at page 5, lines 17-18; *id.* at page 10, lines 20-21.

Claim 38

Claim 38 is directed to a system for communication on a chip. *E.g.*, specification at page 1, line 22; *id.* at page 10, lines 18-21.

The system includes means for communicating between a plurality of on-chip components and a plurality of stations coupled to the plurality of on-chip components. *E.g.*, specification at page 4, lines 2-4; *id.* at page 10, lines 19-20; *id.* at page 18, lines 3-21; *id.* at page 20, line 23 through page 24, line 2; Figure 1, connectors between components 2-11 and their respective stations 13-22; Figure 6 (including arbiter 104, multiplexor 106, and decoder 105); Figure 7, steps S701 and S709. A station is a port to an on-chip communication bus. *E.g.*, specification at page 8, line 7.

The system further includes means for communicating between the plurality of stations using an on-chip communication bus including a plurality of tracks. *E.g.*, specification at page 4, line 2; *id.* at page 9, line 21; *id.* at page 11, line 1 through page 12, line 7; Figure 2, elements 31-34, 36-39, 41-44, and 46-49; Figure 3, elements 57 and 58; Figure 4, elements 79-82; Figure 5, elements 84-87 and 94-97; Figure 8, elements 108-111, 113-117, and 119-126. A track may include lines for data bits and control information. *E.g.*, specification at page 10, lines 1-4.

Each station has a dedicated track which it can use to send information to other stations. *E.g.*, specification at page 10, lines 20-21.

A. Dependent Claims

Claim 4

Claim 4 depends from claim 1. In accordance with claim 4, each station of the system of claim 1 includes an initiator that requests permission to transmit outgoing data over a track to another station and that transmits the outgoing data. *E.g.*, specification at page 13, lines 8-10; Figure 3, element 54; and Figure 4, elements 69-72.

Each station also includes an arbiter that evaluates requests from other stations and selects a track on which to receive incoming data. *E.g.*, specification at page 13, lines 8-11; Figure 3, element 55; Figure 5, elements 84-87.

Each station further includes a target that receives the incoming data. *E.g.*, specification at page 13, lines 8-11; Figure 3, element 56; Figure 4, elements 74-77.

Claim 40

Claim 40 depends from claim 1. In accordance with claim 40, each station includes an arbiter circuit capable of receiving a request signal (a request to send information) and granting permission to a station that originated the request signal to send information to the station that granted permission over the dedicated track of the station that originated the request signal. *E.g.*, specification at page 4, lines 13-17; *id.* at page 11, lines 5-9; *id.* at page 12, lines 1-5; *id.* at page 13, lines 8-11; *id.* at page 16, line 24 through page 17, line 2; *id.* at page 17, lines 7-10; *id.* at page 18, lines 18-19; *id.* at page 21, lines 4-23.

Claims 15 and 34

Claim 15 depends from claim 1 and is directed to a system for communication on a chip. Claim 34 depends from claim 19 and is directed to a method for communication on a chip. In accordance with each of claims 15 and 34, more than one of the plurality of on-chip components are coupled to the on-chip communication bus through one of the stations. *E.g.*, specification at page 18, line 1 through page 19, line 3; Figure 6.

VI
CONCISE STATEMENT OF THE GROUNDS OF REJECTION

1. Claims 1-16, 19-35, and 38 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Carey, U.S. Patent Number 6,460,174 ("Carey" hereinafter). It appears that claims 39-42 have also been rejected on the same ground.[1]

2. Claims 17, 18, 36, and 37 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Carey in view of Adams *et al.*, U.S. Patent Publication Number 2001/0042147 ("Adams" hereinafter).

VII
ARGUMENT

A. Rejection of Independent Claims 1, 19, and 38 as Being Anticipated by Carey

Each of the independent claims 1, 19, and 38 recites the limitation of "wherein each station has a dedicated track which it can use to send information to other stations." The Final Office Action cited Carey at column 2, lines 29-30, as disclosing this limitation. Carey's cited text reads as follows:

> The distributed routing network 4 can be a series of dedicated connections, one or more shared connections or a mixture of dedicated and shared connections. One example of a shared connection is a bus.

[1] The Final Office Action does not expressly state that claims 39-42 are rejected under 35 U.S.C. § 102(e) as being anticipated by Carey, but these claims are discussed under the same heading as the other claims rejected under 35 U.S.C. § 102, and the discussion of the rejections of claims 39-42 does not mention any prior art other than Carey. Applicants therefore proceed on the assumption that claims 39-42 stand rejected as being anticipated by Carey.

Carey, col. 2, lines 28-32. While the cited text gives one example of a "shared connection" – a bus – it does not explain what constitutes a "dedicated connection." The undersigned attorney has searched for such a description throughout Carey, but has not identified a single additional instance of the word "dedicated" in that document. It appears that Carey's description of a "dedicated connection" is limited to contrasting "dedicated connection" to "shared connection," such as a bus. The text quoted above appears to be the sum total of Carey's teaching of "dedicated connection."

Some guidance regarding the meaning of "dedicated connection" may be obtained from Carey's description of the routing network used in the integrated circuit described in that document. In particular, Carey describes Request Transport and Response Transport blocks 34 and 35. Each of these blocks can be a "shared bus" or a "fully connected cross bar." Carey, col. 13, lines 44-50; and col. 14, lines 26-31. One definition of a cross bar (cross-bar) appears below:

> In a network, a cross-bar switch is a device that is capable of channeling data between any two devices that are attached to it up to its maximum number of ports. The paths set up between devices can be fixed for some duration or changed when desired and each device-to-device path (going through the switch) is usually fixed for some period.
>
> Cross-bar topology can be contrasted with bus topology, an arrangement in which there is only one path that all devices share. Traditionally, computers have been connected to storage devices with a large bus. A major advantage of cross-bar switching is that, as the traffic between any two devices increases, it does not affect traffic between other devices. In addition to offering more flexibility, a cross-bar switch environment offers greater scalability than a bus environment.

Techtarget networking dictionary, available (as of the time of this writing) on line at http://whatis.techtarget.com/gDefinition/0%2C294236%2Csid7_gci538079%2C00.html.

Carey does not expressly state that the series of dedicated connections briefly mentioned in column 2, lines 28-32, is in effect a crossbar. But the remainder of that document suggests that this may indeed be the correct interpretation. Specifically, Carey contrasts a shared bus with both dedicated connection and crossbar, and makes multiple references to routing resources, connect resources, and interconnect resource. In any event, Carey apparently does not provide other suggestions as to the meaning of "dedicated connection" in the particular context. As noted above, Carey also does not expressly explain the meaning of "dedicated connection."

The independent claims of the present application use identical verbiage to recite the dedicated track limitation: "wherein each station has a dedicated track which it can use to send information to other stations." The meaning of the adjective "dedicated" can be found in most English dictionaries. The shorter Oxford dictionary defines "dedicated," in a somewhat circular fashion, as something "[t]hat has been dedicated." OXFORD UNIVERSITY PRESS, THE NEW SHORTER OXFORD *ENGLISH DICTIONARY* (CD-ROM ed. 1996). With specific reference to computing machinery, the same dictionary defines the word dedicated as "(designed and) used exclusively for a particular purpose or by a particular user." *Id.* Another general purpose dictionary defines dedicated as "given over to a particular purpose." MERRIAM-WEBSTER'S COLLEGIATE DICTIONARY (Elec. Ed., Ver. 1.2, 1994-96). A computer dictionary gives the following definition of the word "dedicated": "Of, pertaining to, or being a device, program, or procedure devoted to a single task or function." COMPUTER DICTIONARY 150 (Microsoft, 5th ed., 2002). In sum, "dedicated" can be understood to refer generally to something designed for or committed to a single use, task, function, or purpose.

Note that the independent claims recite "dedicated track" not in the abstract, but in association with a station. In accordance with each of these independent claims, a dedicated track is therefore a track dedicated to the specific station.

In contrast, Carey does not teach that each of the dedicated connections is dedicated to a specific station.

Carey also does not teach that "each station has a dedicated track which it can use to send information to other stations," as is recited in each independent claim of the application. For example, Carey does not teach that each station (of some plurality of stations) has a dedicated track. As another example, Carey does not teach that that the dedicated track of a particular station is used to send information from the particular station, rather than receive information at the particular station. Moreover, Carey does not teach that the dedicated track of a particular station connects the particular station to other stations – multiple other stations – rather than to a single other station. In Carey, we simply cannot tell (1) to what device, use, task, function, or purpose each connection is dedicated, (2) whether each connection is a dedicated input or output connection, and (3) whether each dedicated connection is a one-to-one, one-to-many, or many-to-one connection. In contrast, each of the pending independent claims in effect recites that (1) there are a plurality of stations, each with a dedicated track; (2) each station with a dedicated track can use the dedicated track to send information, and (3) each station can use the dedicated track to send information to stations, *i.e.*, to a plurality of stations.

In responding to these arguments, the Final Office Action, at page 8, apparently admits that "Carey does not provide additional details of the 'dedicated connection.'" The Final Office Action then goes on to state that "for the purpose of rejection, and considering the admittedly well-known concept of a dedicated track, this disclosure of Casey is considered adequate to anticipate the claimed dedicated feature." *Id.* For the following reasons we take issue with this argument.

Initially, note that Applicants have not admitted that the concept of a dedicated track is well-known. We have argued and continue to argue that the word "dedicated" has a well defined meaning. Based on this meaning, a person skilled in the art, <u>after perusal of the present application</u>, would understand the concept of "dedicated track." Indeed, if the admission had been made – and it had not – it would be of no consequence because the rejection in issue here was entered for anticipation under section 102, not for obviousness under section 103. If a single prior art reference, such as Carey here, does not expressly or inherently disclose all of the limitations in a claim, the claim is not anticipated by the reference, regardless of what is well-known in the art.

Moreover, Applicants have previously argued that the concept of dedicated track as it is recited in the claims is not well known in the art, traversing the rejections. After applicants adequately traverse the assertion of Official Notice that certain facts are well known in the art, documentary evidence supporting the assertion must be provided in the next Office action if the rejection is to be maintained. MPEP § 2144.03(C). This has not been done in the Advisory Action. Instead, the Advisory Action argues that

> Carey's disclosure of "dedicated connections" adequately anticipates the Applicant's "dedicated track". No further details are necessary to anticipate this feature as it is claimed in the instant invention.
>
> * * *
>
> The "series of dedicated connections" taught by Carey is considered to anticipate the instant invention comprising "each station has a dedicated track".

Advisory Action at page 2.

Given the lack of any explicit description of "dedicated connections" in Carey beyond a bare mention of such connections, Carey cannot anticipate this feature. Furthermore, neither the Final Office Action nor any other Office action issued in this case even attempts to point out where Carey purportedly explains (1) that the connections are <u>dedicated to the stations</u>, (2) that the station to which a connection is dedicated is used by the station to <u>send</u> information, or (3) that each station can use the connection dedicated to the station to send information to a <u>plurality</u> of stations. Carey does not expressly teach these limitations, and the limitations are not inherent in Carey's apparatus.

To anticipate a claim, "[t]he identical invention must be shown in as complete detail as is contained in the . . . claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989) (*quoted with approval in* MPEP § 2131). Carey fails to teach the limitations of "wherein each station has a dedicated track which it can use to send information to other stations." Without this teaching, Carey cannot anticipate independent claims 1, 19, and 38.

B. Rejection of Claim 4 as Being Anticipated by Carey

According to claim 4, each station includes "an arbiter that evaluates requests from other stations and selects a track on which to receive incoming data." The Final Office Action cites Carey at column 2, lines 52-57 for disclosure of this limitation. The cited text, however, states that the "central control logic arbitrates between the requests of the initiator ports 8 to determine which one or more requests are allowed onto the distributed routing network." Carey, col. 2, lines 52-54. Note that the central control logic is depicted in Carey's Figure 1 as an element that is separate from the modules 6. Thus, Carey does not disclose a station or a module that includes an arbiter that selects a track. Instead, Carey describes central control logic that arbitrates between or among requests.

In responding to the Appellants' arguments regarding claim 4, the Final Office Action (at page 8) states that in making arbitration decisions Carey's arbiter uses information regarding the initiator making the request, number of outstanding requests, and target availability, citing Carey at column 13, lines 1-10. The Final Office Action apparently concludes that an arbiter is *assigned* to each station. Applicants respectfully disagree with this rejection for the following reasons.

First, claim 4 recites a plurality of stations wherein each station includes an arbiter. Thus, the system of claim 4 has a plurality of arbiters. Carey teaches a single, centrally located arbiter. *E.g.*, Carey, col. 13, line 1; *id.* Figure 2. Even if the arbiter 38 could have distributed architecture, Carey does not disclose such architecture. To the contrary, Carey specifically states that arbitration is performed by "central control logic." Carey, col. 2, lines 52-55. Carey has chosen to add the adjective "central" to the control logic element that performs the arbitration function, and depicted the element as a separate block in the block diagram of Figure 1. Furthermore, the fact that the

arbiter 38 can use information regarding the number of outstanding requests and target availability does not imply that a separate arbiter circuit is built into each target. For example, the target could send to the central arbiter a signal indicating whether the target is available. Such target need not provide arbitration functions; there could still be a single, centrally located arbiter, as in fact is shown in Carey. Carey does not anticipate claim 4 because Carey does not disclose a plurality of arbiters.

The Final Office Action in fact admits, at page 8, that Carey's "arbitration is centrally located." The Final Office Action then notes, also at page 8, that because the arbitration decisions are made based on target availability, "it can be determined that if the target is available for arbitration, then arbitration is done." Applicants understood this to mean that the Final Office Action treats <u>a target's input to the central arbiter</u> as a <u>separate arbiter</u> at the target or station. An arbiter, however, is more than an input or output. It is a circuit that actually performs the arbitration function. Specifically, claim 4 recites "an arbiter that evaluates requests . . . and selects a track." This is not a mere input to some central logic that performs arbitration in Carey's apparatus.

Carey teaches a single, centrally located arbiter 38. *E.g.*, Carey, col. 13, line 1; *id.* Figure 2. Even if the arbiter 38 could have distributed architecture, Carey does not disclose such architecture, at least Carey does not disclose more than receiving information regarding target availability from the targets. A <u>single central arbiter</u> is not necessarily transformed into a <u>plurality of distributed arbiters</u> by the mere fact that it receives multiple inputs regarding availability of targets. A hypothetical circuit that performs some function is not necessarily transformed into a plurality of circuits simply because the circuit has a plurality of inputs. According to claim 4, each station

includes an arbiter. Carey does not anticipate claim 4 because it discloses a single, central arbiter, instead of an arbiter at each of a plurality of stations.

Second, even if a centrally-located arbiter is "assigned" to a station, it is not necessarily "comprised" or "included" in the station. As defined in the specification, a station is a "port to an on-chip communication bus according to the invention." Specification, at page 8, line 7. Some degree of co-location of various constituent components of the station should be present. In other words, claim 4 reciting a station that includes an arbiter is not identical to a hypothetical claim that would recite a system *further comprising an arbiter assigned to each station.* Because Carey's central control logic arbiter is not included in each station, Carey does not anticipate claim 4.

C. Rejection of Claim 40 as Being Anticipated by Carey

According to claim 40, "each station includes an arbiter circuit capable of receiving a request signal and granting permission to a station that originated the request signal to send information to the station that granted permission over the dedicated track of the station that originated the request signal." Claim 40 is not anticipated by Carey for the reasons discussed in the immediately preceding section in relation to claim 4. Moreover, claim 40 expressly recites an arbiter circuit at each station. Even assuming that Carey discloses an input or connection from the target to the central arbiter, a "circuit" is more than a mere input or connection.

D. Rejection of Claims 15 and 34 as Being Anticipated by Carey

Claims 15 and 34 recite more than one component being coupled to the communication bus through one station. This arrangement is illustrated, for example, in Figure 6 of the present application. The Final Office Action states that Carey teaches this limitation at column 2, lines 36-39. The cited text, however, merely states that modules can be of any form. It does not teach that multiple components are connected to the bus using the same station, *i.e.*, using the same port to the bus[2] or the same module.

In response to this argument, the Final Office Action states, at page 9, that "[w]hat constitutes a component is not recited," and broadly interprets component "as some item that is addressable beyond the addressing of the port itself." The Office Action cites Carey at column 4, lines 40-49, as teaching this limitation. The interpretation of the term "component" by the Office Action is overbroad.

The present application does in fact define the term "component":

> Component: A subset of circuits on a chip that perform a particular function or operation. Examples include, but are not limited to, a PCI (peripheral component interconnect) bridge, a USB (universal serial bus) interface, an I2C (inter-integrated-circuit) interface, a UART (universal asynchronous receiver transmitter) interface, a DDR (data direction register) and/or SDRAM (synchronous dynamic access memory), an ethernet interface, a general I/O (input/output) interface, and other circuits and interfaces. Components also can be referred to as peripherals.

Application, page 7, line 23, through page 8, line 5. Although the definition does not limit a "component" to the specific components listed, it does limit a component to a "subset of circuits on a

[2] The present application defines a station as a "port to an on-chip communication bus according to the invention," at page 8, line 7.

chip that perform a particular function or operation." Therefore, a component is a functional or operational component. It is not merely an addressable location. Carey does not teach multiple functional/operational components coupled to the bus through one station. For this reason, claims 15 and 34 are separately patentable over Carey.

Moreover, the Final Office Action applies an incorrect legal standard to determining whether Carey anticipates claims 15 and 34. The Final Office Action purports "[t]o determine whether Carey discloses some equivalent" of the limitation in claims 15 and 34. Final Office Action, page 9, lines 9-10 (underlining added for emphasis). Equivalence should not be considered in determining anticipation under section 102. The issue is whether Carey discloses the "identical invention . . . in as complete detail as is contained in the . . . claim." *Richardson, supra*, 868 F.2d 1236, 9 U.S.P.Q.2d 1920. Because Carey does not disclose an identical invention, Carey does not anticipate claims 15 and 34.

E. Rejection of Remaining Dependent Claims

Dependent claims not specifically addressed in the above arguments should be patentable at least for the reasons discussed in relation to their base and intervening claims.

VIII
CONCLUSION

For the foregoing reasons, Appellants respectfully submit that all pending claims are patentable over references of record and respectfully requests reversal of the rejections.

Respectfully submitted,

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Anatoly S. Weiser
Reg. No. 43,229

The Swernofsky Law Group
P.O. Box 390013
Mountain View, CA 94039-0013
(650) 947-0700

APPENDIX – CLAIMS ON APPEAL

The following is a listing of the claims in the application. All claims 1-42 have been rejected and are involved in this Appeal.

1. (Original): A system for communication on a chip, comprising:

an on-chip communication bus including plural tracks; and

a plurality of stations that couple a plurality of on-chip components to the on-chip communication bus;

wherein each station has a dedicated track which it can use to send information to other stations.

2. (Original): A system as in claim 1, wherein the stations use a packet based communication protocol.

3. (Original): A system as in claim 1, wherein the on-chip components include a PCI bridge, a USB component, or an inter-integrated-circuit component.

4. (Original): A system as in claim 1, wherein each station includes:

an initiator that requests permission to transmit outgoing data over a track to another station and that transmits the outgoing data;

an arbiter that evaluates requests from other stations and selects a track on which to receive incoming data; and

a target that receives the incoming data.

5. (Original): A system as in claim 4, wherein the initiator is connected to a grant multiplexor for selecting a grant line.

6. (Original): A system as in claim 5, wherein the grant multiplexor further comprises plural smaller multiplexors distributed across the chip.

7. (Original): A system as in claim 4, wherein the arbiter is connected to a track multiplexor for selecting a track.

8. (Original): A system as in claim 7, wherein the track multiplexor further comprises plural smaller multiplexors distributed across the chip.

9. (Original): A system as in claim 4, wherein each station further comprises a source queue for queuing outgoing data.

10. (Original): A system as in claim 9, wherein the source queue is a first-in-first-out register.

11. (Original): A system as in claim 4, wherein each station further comprises a destination queue for queuing incoming data.

12. (Original): A system as in claim 11, wherein the destination queue is a first-in-first-out register.

13. (Original): A system as in claim 4, wherein each station further comprises:

a source queue for queuing outgoing data, and

a destination queue for queuing incoming data.

14. (Original): A system as in claim 13, wherein the source queue and the destination queue serve to separate a first clock domain for the on-chip communication bus from a second clock domain for one of the plurality of on-chip components.

15. (Original): A system as in claim 1, wherein more than one of the plurality of on-chip components are coupled to the on-chip communication bus through one of the stations.

16. (Original): A system as in claim 1, wherein the stations comprise multiplexors that further comprise:

smaller multiplexors distributed across the chip in stages;

pipeline storage elements between some of the stages in order to maintain transmission speed when a track must traverse a large number of stages.

17. (Original): A system as in claim 1, wherein each station comprises a watchdog circuit that determines if its station has gone offline.

18. (Previously Presented): A system as in claim 17, wherein if the watchdog circuit determines that its station has gone offline, that watchdog circuit informs a controller connected to the system.

19. (Original): A method for communication on a chip, comprising the steps of:

communicating between a plurality of on-chip components and a plurality of stations coupled to the plurality of on-chip components; and

communicating between the plurality of stations using an on-chip communication bus including a plurality of tracks;

wherein each station has a dedicated track which it can use to send information to other stations.

20. (Original): A method as in claim 19, wherein the stations use a packet based communication protocol.

21. (Original): A method as in claim 19, wherein the on-chip components include a PCI bridge, a USB component, or an inter-integrated-circuit component.

22. (Original): A method as in claim 19, wherein the step of communicating between the plurality of stations further comprises the steps of:

sending a request from a first station to a second station;

evaluating the request at the second station;

sending a grant signal from the second station to the first station;

selecting a track at the second station;

sending a data or command from the first station to the second station; and

receiving the data or command at the second station.

23. (Original): A method as in claim 22, wherein

sending the request is performed by an initiator at the first station;

evaluating the request is performed by an arbiter at the second station;

sending the grant signal is performed by the arbiter at the second station;

selecting the track is performed by the arbiter at the second station;

sending the data or command is performed by the initiator at the first station; and

receiving the data is performed by a target at the second station.

24. (Original): A method as in claim 23, wherein the initiator is connected to a grant multiplexor for selecting a grant line.

25. (Previously Presented): A method as in claim 24, wherein the grant multiplexor comprises plural smaller multiplexors distributed across the chip.

26. (Original): A method as in claim 23, wherein the arbiter is connected to a track multiplexor for selecting a track.

27. (Previously Presented): A method as in claim 26, wherein the track multiplexor comprises plural smaller multiplexors distributed across the chip.

28. (Original): A method as in claim 23, wherein each station further comprises a source queue for queuing outgoing data.

29. (Original): A method as in claim 28, wherein the source queue is a first-in-first-out register.

30. (Original): A method as in claim 23, wherein each station further comprises a destination queue for queuing incoming data.

31. (Original): A method as in claim 30, wherein the destination queue is a first-in-first-out register.

32. (Original): A method as in claim 23, wherein each station further comprises:

a source queue for queuing outgoing data, and

a destination queue for queuing incoming data.

33. (Original): A method as in claim 32, wherein the source queue and the destination queue serve to separate a first clock domain for the on-chip communication bus from a second clock domain for one of the plurality of on-chip components.

34. (Original): A method as in claim 19, wherein more than one of the plurality of on-chip components are coupled to the on-chip communication bus through one of the stations.

35. (Original): A method as in claim 19, wherein the stations comprise multiplexors that further comprise smaller multiplexors distributed across the chip in stages and pipeline storage elements between some of the stages in order to maintain transmission speed when a track must traverse a large number of stages.

36. (Original): A method as in claim 19, further comprising the step of determining if a station has gone offline, the step of determining performed by a watchdog circuit for the station.

37. (Original): A method as in claim 36, further comprising the step of informing a controller if the watchdog circuit determines that its station has gone offline.

38. (Original): A system for communication on a chip, comprising:

means for communicating between a plurality of on-chip components and a plurality of stations coupled to the plurality of on-chip components; and

means for communicating between the plurality of stations using an on-chip communication bus including a plurality of tracks;

wherein each station has a dedicated track which it can use to send information to other stations.

39. (Previously Presented) A system as in claim 1, wherein each station comprises a requester circuit capable of sending a request signal requesting grant of use of one of the dedicated tracks for communication with other stations, wherein the request signal incorporates one of a plurality of priority levels.

40. (Previously Presented) A system as in claim 1, wherein each station includes an arbiter circuit capable of receiving a request signal and granting permission to a station that originated the request signal to send information to the station that granted permission over the dedicated track of the station that originated the request signal.

41. (Previously Presented) A system as in claim 40, wherein the request signal incorporates a request priority level, and the arbiter circuit is capable of granting permission based on the request priority level.

42. (Previously Presented) A system as in claim 40, wherein the arbiter circuit is directly connected to at least a subset of the plurality of stations to receive request signals from the stations of the subset, the subset comprising the station that originated the request signal.